CLAIM AMENDMENTS

1 (Currently Amended). A sample/hold circuit, comprising:

an amplifier having an output for providing an output of said sample/hold circuit;

a first capacitor for sampling a value of an input signal during a first sampling phase of a sample clock;

a second capacitor for sampling a value of said input signal during a second sampling phase of said sample clock; and

a switching circuit for alternatively selecting one of said first capacitor and said second capacitor for coupling to said ~~said~~ input signal during each phase of said sample clock, wherein another one of said first capacitor and said second capacitor not selected for coupling to said input signal is coupled between said output of said amplifier and an input of said amplifier for holding a value at an output of said amplifier sampled during a previous phase of said sample clock, whereby each of said first capacitor and said second capacitor alternates between sampling said input signal and holding said value in a mutually-exclusive manner, whereby transitions in said output of said amplifier are reduced between sampling intervals of said sample/hold;

wherein said switching circuit further comprises at least one input bootstrap clock circuit coupled to said switching circuit for generating a control signal having an on-state control voltage derived in conformity with a voltage level of said input signal, whereby the on-state of a control voltage input of at least one switch that couples said first capacitor to said input signal is maintained at a substantially constant level with respect to said input signal.

2 (Currently Amended). The sample/hold circuit of Claim 1, wherein said input signal is a differential input signal pair, wherein said amplifier is a fully differential amplifier having a differential amplifier input pair and a differential output pair for providing a differential output of said sample/hold, wherein said first and second capacitor are alternatively and mutually-exclusively coupled to one of a first input of said differential input pair and a feedback position between a first output of said differential output pair and a first one of said differential amplifier input pair, and wherein said sample/hold circuit further comprises:

a third capacitor for sampling a value of said input signal during said first phase of said sample clock; and

a fourth capacitor for sampling a value of said input signal during said second phase of said sample clock, and wherein said switching circuit alternatively selects one of said third capacitor and said fourth capacitor for coupling to a second one of said differential input signal pair during each phase of said sample clock, wherein another one of said third capacitor and said fourth capacitor not selected for coupling to said second differential input signal is coupled between said ~~a~~ second output of said differential output pair and ~~a~~ said second one of said differential amplifier input pair for holding said value at an output of said amplifier obtained in conformity with a previous phase of said sample clock, whereby each of said third capacitor and said fourth capacitor alternates between sampling said input signal and holding said value in a mutually-exclusive manner.

3 (Original). The sample/hold circuit of Claim 2, wherein said switching circuit further comprises at least one input bootstrap clock circuit coupled to said switching circuit for generating a control signal having an on-state control voltage derived in conformity with a voltage level of said input signal, whereby the on-state of a control voltage input of at least one switch that couples said first capacitor to said input signal is maintained at a substantially constant level with respect to said input signal.

4 (Original). The sample/hold circuit of Claim 3, wherein said switching circuit further comprises at least one output bootstrap clock circuit coupled to said switching circuit for generating a control signal having an on-state control voltage derived in conformity with a voltage level of said amplifier output signal, whereby the on-state of a control voltage input of at least one switch that couples said first capacitor to said amplifier output is maintained at a substantially constant level with respect to said amplifier output signal.

5 (Original). The sample/hold circuit of Claim 2, wherein said switching circuit further comprises:

a first shunt switch for shorting a first common-mode terminal of said first capacitor to a third common-mode terminal of said third capacitor; and

a second shunt switch for shorting a second common-mode terminal of said second capacitor to a fourth common-mode terminal of said fourth capacitor, and wherein said switching circuit is coupled to control inputs of said first shunt switch and said second shunt switch for further reducing deviations between terminals of said first capacitor, said second capacitor, said third capacitor and said fourth capacitor while coupled to a common mode voltage of said sample/hold circuit.

6 (Cancelled).

7 (Currently Amended). The sample/hold circuit of Claim 1 ~~6~~, wherein said bootstrap clock circuit comprises:

a boost capacitor having a first terminal selectively coupled to said control voltage input of said at least one switch;

a charging circuit coupled to said first terminal of said boost capacitor for charging said boost capacitor to a predetermined constant voltage level; and

a transmission gate for transferring said voltage level of said input signal to a second terminal of said boost capacitor prior to said coupling of said first terminal of said capacitor to said control voltage input of said at least one switch, whereby said first terminal of said boost capacitor is raised to a voltage level substantially equal to said predetermined constant voltage level plus said voltage level of said input signal.

8 (Currently Amended). A sample/hold circuit, comprising:

an amplifier having an output for providing an output of said sample/hold circuit;

a first capacitor for sampling a value of an input signal during a first sampling phase of a sample clock;

a second capacitor for sampling a value of said input signal during a second sampling phase of said sample clock; and

a switching circuit for alternatively selecting one of said first capacitor and said second capacitor for coupling to said ~~said~~ input signal during each phase of said sample clock, wherein another one of said first capacitor and said second capacitor not selected for coupling to said input signal is coupled between said output of said amplifier and an input of said amplifier for holding a value at an output of said amplifier sampled during a previous phase of said sample clock, whereby each of said first capacitor and said second capacitor alternates between sampling said input signal and holding said value in a mutually-exclusive manner, whereby transitions in said output of said amplifier are reduced between sampling intervals of said sample/hold;

~~The sample/hold circuit of Claim 1,~~ wherein said switching circuit further comprises at least one output bootstrap clock circuit coupled to said switching circuit for generating a control signal having an on-state control voltage derived in conformity with a voltage level of said amplifier output signal, whereby the on-state of a control voltage input of at least one switch that couples said first capacitor to said amplifier output is maintained at a substantially constant level with respect to said amplifier output signal.

9 (Original). The sample/hold circuit of Claim 5, wherein said bootstrap clock circuit comprises:

a boost capacitor having a first terminal selectively coupled to said control voltage input of said at least one switch;

a charging circuit coupled to said first terminal of said boost capacitor for charging said boost capacitor to a predetermined constant voltage level; and

a transmission gate for transferring said voltage level of said amplifier output signal to a second terminal of said boost capacitor prior to said coupling of said first terminal of said capacitor to said control voltage input of said at least one switch, whereby said first terminal of said boost capacitor is raised to a voltage level substantially equal to said predetermined constant voltage level plus said voltage level of said amplifier output signal.

10 (Currently Amended). A sample/hold circuit, comprising:

an amplifier having a first output for providing a first output of said sample/hold circuit, an inverting input and a non-inverting input;

a first capacitor;

a first transistor having a first channel terminal connected to an input voltage of said sample/hold and a second channel terminal connected to a first terminal of said first capacitor;

a second transistor having a first channel terminal connected to a reference voltage of said sample/hold and a second channel terminal connected to a second terminal of said first capacitor;

a third transistor having a first channel terminal connected to said inverting input of said amplifier and a second channel terminal connected to said second terminal of said first capacitor;

a fourth transistor having a first channel terminal connected to said first amplifier output and a second channel terminal connected to ~~a second~~ said first terminal of said first capacitor;

a second capacitor;

a fifth transistor having a first channel terminal connected to an input voltage of said sample/hold and a second channel terminal connected to a first terminal of said second capacitor;

a sixth transistor having a first channel terminal connected to said reference voltage and a second channel terminal connected to a second terminal of said second capacitor;

a seventh transistor having a first channel terminal connected to said inverting input of said amplifier and a second channel terminal connected to said second terminal of said second capacitor;

an eighth transistor having a first channel terminal connected to said first amplifier output and a second channel terminal connected to ~~a second~~ said first terminal of said second capacitor; ~~and~~

a switching control circuit coupled to gates of all of said transistors for alternating said first capacitor and said second capacitor in a mutually exclusive manner by enabling said first, second, seventh and eighth transistors in alternation with said third, fourth, fifth and sixth transistors;

a boost capacitor;

a boost transistor having a first channel terminal connected to a gate of said first transistor and a second channel terminal coupled to a first terminal of said boost capacitor;

a transmission gate coupled to a second terminal of said boost capacitor and said input of said sample/hold circuit; and

a charging circuit for charging said boost capacitor to a predetermined voltage level, and wherein said switching circuit selectively enables said transmission gate and said boost transistor when said first transistor is initially enabled, whereby a gate voltage of said first transistor is boosted in conformity with a value of said input signal.

11 (Currently Amended). The sample/hold circuit of Claim 10, wherein said amplifier is a differential amplifier, wherein said first output of said amplifier is a non-inverted output and wherein said differential amplifier further has an inverted output, and wherein said circuit further comprises:

a third capacitor;

a ninth transistor having a first channel terminal connected to an inverted input voltage of said sample/hold and a second channel terminal connected to a first terminal of said third capacitor;

a tenth transistor having a first channel terminal connected to said reference voltage of said sample/hold and a second channel terminal connected to a second terminal of said third capacitor;

an eleventh transistor having a first channel terminal connected to said non-inverting input of said amplifier and a second channel terminal connected to said second terminal of said third capacitor;

a twelfth transistor having a first channel terminal connected to said inverted amplifier output and a second channel terminal connected to ~~a second~~ said first terminal of said third capacitor;

a fourth capacitor;

a thirteenth transistor having a first channel terminal connected to said inverted input voltage and a second channel terminal connected to a first terminal of said fourth capacitor;

a fourteenth transistor having a first channel terminal connected to said reference voltage and a second channel terminal connected to a second terminal of said fourth capacitor;

a fifteenth transistor having a first channel terminal connected to said non-inverting input of said amplifier and a second channel terminal connected to said second terminal of said fourth capacitor; and

a sixteenth transistor having a first channel terminal connected to said inverted amplifier output and a second channel terminal connected to ~~a second~~ said first terminal of said fourth capacitor, and wherein said switching control circuit is further coupled to gates of said ninth, tenth, eleventh, twelfth, thirteenth, fourteenth, fifteenth and sixteenth ~~sixteenth~~ transistors for alternating said third capacitor and said fourth capacitor in a mutually exclusive manner by enabling said ninth, tenth, fifteenth and sixteenth transistors in alternation with said eleventh, twelfth, thirteenth and fourteenth transistors.

12 (Original). The sample/hold circuit of Claim 11, further comprising:

a seventeenth transistor having a first channel connection connected to said second terminal of said first capacitor, a second channel connection connected to said second terminal of said third capacitor, and a gate coupled to said switching control circuit, whereby said switching control circuit enables said seventeenth transistor while said second and tenth transistors are enabled, whereby a difference of voltages on said second terminals of said first capacitor and said third capacitor are reduced; and

an eighteenth transistor having a first channel connection connected to said second terminal of said second capacitor, a second channel connection connected to said second terminal of said fourth capacitor, and a gate coupled to said switching control circuit, whereby said switching control circuit enables said eighteenth transistor while said sixth and fourteenth transistors are enabled, whereby a difference of voltages on said second terminals of said second capacitor and said fourth capacitor are reduced

13 (Cancelled).

14 (Currently Amended). A sample/hold circuit, comprising:

an amplifier having a first output for providing a first output of said sample/hold circuit, an inverting input and a non-inverting input;

a first capacitor;

a first transistor having a first channel terminal connected to an input voltage of said sample/hold and a second channel terminal connected to a first terminal of said first capacitor;

a second transistor having a first channel terminal connected to a reference voltage of said sample/hold and a second channel terminal connected to a second terminal of said first capacitor;

a third transistor having a first channel terminal connected to said inverting input of said amplifier and a second channel terminal connected to said second terminal of said first capacitor;

a fourth transistor having a first channel terminal connected to said first amplifier output and a second channel terminal connected to said first terminal of said first capacitor;

a second capacitor;

a fifth transistor having a first channel terminal connected to an input voltage of said sample/hold and a second channel terminal connected to a first terminal of said second capacitor;

a sixth transistor having a first channel terminal connected to said reference voltage and a second channel terminal connected to a second terminal of said second capacitor;

a seventh transistor having a first channel terminal connected to said inverting input of said amplifier and a second channel terminal connected to said second terminal of said second capacitor;

an eighth transistor having a first channel terminal connected to said first amplifier output and a second channel terminal connected to said first terminal of said second capacitor; ~~and~~

a switching control circuit coupled to gates of all of said transistors for alternating said first capacitor and said second capacitor in a mutually exclusive manner by enabling said first, second, seventh and eighth transistors in alternation with said third, fourth, fifth and sixth transistors;

~~The sample/hold circuit of Claim 10, further comprising~~

a boost capacitor;

a boost transistor having a first channel terminal connected to a gate of said fourth transistor and a second channel terminal coupled to a first terminal of said boost capacitor;

a transmission gate coupled to a second terminal of said boost capacitor and said input of said sample/hold circuit; and

a charging circuit for charging said boost capacitor to a predetermined voltage level, and wherein said switching circuit selectively enables said transmission gate and said boost transistor when said fourth transistor is initially enabled, whereby a gate voltage of said fourth transistor is boosted in conformity with a value of said amplifier output.

15 (Currently Amended). A method of sampling an input voltage, comprising:

first alternating a first capacitor between a first sampling position for charging said first capacitor to said input voltage and a first hold position for holding an output voltage of an amplifier; and

second alternating a second capacitor between a second sampling position for charging said second capacitor to said input voltage and a second hold position for holding said output voltage of said amplifier, wherein said second alternating is performed in an opposite phase of said sampling from said first alternating.

boosting a control voltage of a switch performing said first alternating during said first sampling position to a level determined in conformity with said input voltage;

wherein said boosting comprises:

charging a boost capacitor to a predetermined voltage;

selectively coupling a first terminal of said boost capacitor to said input signal; and

selectively coupling a second terminal of said boost capacitor to a control input of a switch performing said first alternating by alternating said first capacitor to said sampling position.

16 (Original). The method of Claim 15, wherein said input signal is a differential input signal pair, wherein said amplifier is a fully differential amplifier having a differential amplifier input pair and a differential output pair for providing a differential output of said sample/hold, wherein said first alternating alternates said first capacitor between said first sampling position for charging said first capacitor to a first input voltage of said differential input signal pair and alternates a third capacitor between a third sampling position for charging said third capacitor to a second input voltage of said differential input signal pair, and wherein said second alternating alternates said second capacitor between said first sampling position for charging said second capacitor to said first input voltage of said differential input signal pair and alternates a fourth capacitor between a fourth sampling position for charging said fourth capacitor to a second input voltage of said differential input signal pair

17 (Cancelled).

18 (Cancelled).

19. A method of sampling an input voltage, comprising:

first alternating a first capacitor between a first sampling position for charging said first capacitor to said input voltage and a first hold position for holding an output voltage of an amplifier; and

second alternating a second capacitor between a second sampling position for charging said second capacitor to said input voltage and a second hold position for holding said output voltage of said amplifier, wherein said second alternating is performed in an opposite phase of said sampling from said first alternating.

boosting a control voltage of a switch performing said first alternating during said first sampling position to a level determined in conformity with said input voltage;

~~The method of Claim 15,~~ wherein said boosting comprises:

charging a boost capacitor to a predetermined voltage;

selectively coupling a first terminal of said boost capacitor to said amplifier output signal; and

selectively coupling a second terminal of said boost capacitor to a control input of a switch performing said first alternating by alternating said first capacitor to said hold position.

20 (Original). The method of Claim 16, further comprising:

shorting a first common-mode terminal of said first capacitor to a third common-mode terminal of said third capacitor only while said first capacitor and said third capacitor are selected by said first alternating to said sample position; and

shorting a second common-mode terminal of said second capacitor to a fourth common-mode terminal of said fourth capacitor only while said first capacitor and said third capacitor are selected by said first alternating to said sample position.